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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/271,503	03/18/1999	KENICHI MORITA	325772008700	4229

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EXAMINER

MITCHELL, MONICA J

ART UNIT

PAPER NUMBER

2622

DATE MAILED: 07/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/271,503

Applicant(s)

MORITA ET AL.

Examiner

Monica J. Mitchell

Art Unit

2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 June 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-15 is/are allowed.
- 6) ☒ Claim(s) 1-7,9,12,16,18 and 19 is/are rejected.
- 7) ☒ Claim(s) 8,10,11 and 17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. This action is in response to the following communications: amendment received June 5, 2003.
2. Claims 1-19 pending.

***Claim Rejections - 35 USC § 112***

3. Claim 19 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The first and second stages, claimed in 19, are not explained in the specification. The processing units are connected to an interface that is connecting them to a network. Examiner doesn't understand the difference between the first and second states if the processing units are connected to the network interface in the first place.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7, 9, 12, 16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al (U.S. Patent Number 4,658,299).

Regarding claim 1, Tanaka discloses an imaging processor comprising: a plurality of function blocks (Figure 2, reference elements 1, 2, 3, 42 and 7) connectable to each other and dealing with image data (column 4, lines 20-26); an interface (Figure 2, reference element 37) connected to a network (column 4, lines 1-6; Fig. 2 shows reference elements 36 and 37 are connected through bus 41, with element 36 being able to communicate with a network); and a bus changer (Figure 2, reference element 9) which changes bus connections among said plurality of function blocks (column 5, line 33-35) and said interface (column 4, lines 5-6).

Regarding claim 2, Tanaka discloses the image processor wherein said plurality of function blocks comprise an image input block which receives image data (column 2, line 67 to column 3, line 3 and column 3, lines 12-17), an image processing block which deals with image data (column 2, line 55 to column 3 line 3 and column 3, lines 12-17), and an image output block which outputs the image data (column 3, lines 4-8).

Regarding claim 3, Tanaka discloses the image processor wherein said image input block receives image data read with an image sensor (column 3, lines 12-17).

Regarding claim 4, Tanaka discloses the image processor wherein said image output block prints an image on a registering medium (column 3, lines 4-8).

Regarding claim 5, Tanaka discloses the image processor wherein said bus changer which is connected to the image input block changes the bus connection such that image data from said network is received through said interface (column 4, lines 30-38; Fig. 2 shows reference elements 36 and 37 are connected through bus 41, with element 36 being able to communicate with a network) sent to said network through

said image output block or said interface (column 4, lines 30-38; Fig. 2 shows reference elements 36 and 37 are connected through bus 41, with element 36 being able to communicate with a network).

Regarding claim 6, Tanaka discloses the image processor wherein one of said function blocks comprises a memory (Figure 2, reference element 33 and 35) which stores an application program (column 3, lines 60-62 and column 3, lines 66-68) and a controller (Figure 2, reference element 32) which processes the image data according to the application program (column 3, lines 60-62).

Regarding claim 7, Tanaka inherently discloses the image processor wherein said memory has a capacity which stores another application program further (column 3, lines 66-68).

Regarding claim 9, Tanaka discloses an imaging processor comprising: a plurality of function blocks (Figure 2, reference elements 1, 2, 3, 42 and 7) connectable to each other and dealing with image data (column 4, lines 20-26); an interface (Figure 2, reference element 37) connected to a network (column 4, lines 1-6; Fig. 2 shows reference elements 36 and 37 are connected through bus 41, with element 36 being able to communicate with a network); a bus changer (Figure 2, reference element 9) which changes bus connections among said plurality of function blocks (column 5, line 33-35) and said interface (column 4, lines 5-6); and a controller (Figure 2, reference element 32) which discriminates data received from said network and controls data transmission to one of the function blocks to be operated (column 4, line 61 to column 5, line 6).

Regarding claim 12, Tanaka discloses the image processor wherein said plurality of function blocks comprise an image input block which receives image data (column 2, line 67 to column 3, line 3 and column 3, lines 12-17), an image processing block which deals with image data (column 2, line 55 to column 3 line 3 and column 3, lines 12-17), and an image output block which outputs the image data (column 3, lines 4-8).

Regarding claim 16, Tanaka discloses a method of controlling image processing in an image processor including a plurality of function blocks, comprising following steps of: receiving a request to perform a function (column 3 lines 55-57); deciding whether the function is executable in said image processor (column 5, lines 3-6); and changing bus connection between a necessary function block and said interface to operate an external apparatus connected through an interface connectable to said network when the function is decided not executable in said image processor (column 4, line 61 to column 5, line 2).

Regarding claim 18, Tanaka discloses the method further comprising the step of sending a signal to request execution of the function to the external image processor (column 4, line 61 to column 5, line 2).

#### ***Allowable Subject Matter***

6. Claims 13-15 are allowed.
7. Claims 8, 10, 11 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Response to Arguments***

8. Applicant's arguments filed 6/5/03 have been fully considered but they are not persuasive.

Applicant submits that the functions blocks, 1, 2, 3, 42, and 7, are not connectable to each other through a network. Applicant's arguments are based on subject matter not being claimed. Claims 1, 9, and 16 simply claims, "an interface connected to a network" and do not claim that the function blocks are connectable to each other through a network.

Applicant also submits the switching unit, element 9, selects destination of image signals but doesn't change bus connections among the plurality of function blocks. Examiner respectfully disagrees. Column 3, lines 33-35 clearly disclose, "a switching unit 9 switches the connections of the input/output stations according to the signals from the control unit".

Applicant also submits that there is no disclosure that teaches or suggests that this CPU 32 receives any data from the network and then controls the data transmission to one of the function blocks to be operated. Again, Examiner respectfully disagrees. Tanaka clearly discloses CPU 32 performing control operations (column 3, lines 61-62) for control unit 1. The control unit 1 comprises a communication interface 36, which receives and transmits data to external apparatuses (column 4, lines 1-6). The control unit 1 then outputs received data to switching unit 9, which then switches connections of the input/output units according to control unit 1 (column 3, lines 33-36). Thus, clearly indicating that CPU 32 controls data transmission to the various blocks. The switching

unit simply transmits data to a particular block based on data received from control unit 1 (column 4, lines 1-39).

Applicant submits that if the function blocks cannot perform the requested function, an external apparatus will be requested to "fill in", however, Tanaka discloses printer unit 7 may be utilized as a secondary printer if printer unit 3 fails (column 3, lines 26-29).

### ***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica J. Mitchell whose telephone number is 703-306-3430. The examiner can normally be reached on Mon.-Fri., 7:30 a.m. to 4:30 p.m..



If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward L. Coles can be reached on 703-305-4712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9313 for regular communications and 703-872-9313 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

mjm  
July 23, 2003

  
EDWARD COLES  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600